WHAT IS CLAIMED IS:

1. A method for providing an increased bit resolution to a data converter operable to convert digital information to analog values, comprising the steps of:

controlling in a first step of controlling a first current Digital-to-Analog (IDAC) converter to provide a first current through a first output node, the first IDAC having a first current step size associated with the Least Significant Bit (LSB) thereof; and

controlling in a second step of controlling a second IDAC to provide a second current through the first output node, the second IDAC having a second current step size associated with the LSB thereof that is smaller than the first current step size;

wherein the current through the first output node is the sum of the first and second currents;

wherein the combination of the first and second IDACs increases the bit resolution of the first IDAC when driving the first output node with the addition of the second IDAC.

2. The method of Claim 1, and further controlling the second IDAC to not provide current to the first output node.

3. The method of Claim 1, wherein the outputs of the first and second steps of controlling are operable to Wire OR the outputs of both of the first and second IDACs to the first output node.

4. The method of Claim 3, wherein the second step of controlling is operable to selectively control the second IDAC to provide current to the first output node in a first and combination mode and to provide current to a second and separate output node in a second and non-combination mode.

5. The method of Claim 1, wherein the first and second IDACs drive current to the first output node in a current sourcing operation.

6. The method of Claim 1, wherein at least one of the first and second IDACs is operable to sink current from the first output node.

7. The method of Claim 1, wherein the first and second IDACs each have a length "n" with there being 2^n levels of current separated by the first current size and second current size, respectively.

8. The method of Claim 7, wherein the combination of the first and second IDACs provides a combined IDAC with a length of $n + \log_2(m)$, wherein m is equal to the ratio of the first step size to the second step size.

9. The method of Claim 7, wherein the second IDAC has a smaller gain than the first IDAC.

10. The method of Claim 7, wherein the second IDAC has a full scale current that is less than the full scale current of the first IDAC.

11. The method of Claim 7, wherein the second IDAC has a smaller gain than the first IDAC and a full scale current that is less than the full scale current of the first IDAC.

12. A method for processing digital data and providing that data to an output as analog data in the analog domain, comprising the steps of:

processing digital data with a central processing unit (CPU);

controlling with the CPU in a first step of controlling a first current Digital-to-Analog (IDAC) converter to convert a first digital value to a first current through a first output node representing an analog value in the analog domain, the first IDAC having a first current step size associated with the Least Significant Bit (LSB) thereof; and

controlling with the CPU in a second step of controlling a second IDAC to convert a second digital value to a second current through the first output node representing an analog value in the analog domain, the second IDAC having a second current step size associated with the LSB thereof that is smaller than the first current step size;

wherein the current through the first output node is the sum of the first and second currents;

wherein the combination of the first and second IDACs increases the bit resolution of the first IDAC when driving the first output node with the addition of the second IDAC.

13. The method of Claim 12, and further controlling the second IDAC with the CPU to not provide current to the first output node.

14. The method of Claim 12, wherein the outputs of the first and second steps of controlling are operable to Wire OR the outputs of both of the first and second IDACs to the first output node.

15. The method of Claim 14, wherein the second step of controlling is operable to selectively control the second IDAC to provide current to the first output node in a first and combination mode and to provide current to a second and separate output node in a second and non-combination mode.

16. The method of Claim 12, wherein the first and second IDACs drive current to the first output node in a current sourcing operation.

17. The method of Claim 12, wherein at least one of the first and second IDACs is operable to sink current from the first output node.

18. The method of Claim 12, wherein the first and second IDACs each have a length "n" with there being 2^n levels of current separated by the first current size and second current size, respectively.

19. The method of Claim 18, wherein the combination of the first and second IDACs provides a combined IDAC with a length of $n + \log_2(m)$, wherein m is equal to the ratio of the first step size to the second step size.

20. The method of Claim 18, wherein the second IDAC has a smaller gain than the first IDAC.

21. The method of Claim 18, wherein the second IDAC has a full scale current that is less than the full scale current of the first IDAC.

22. The method of Claim 18, wherein the second IDAC has a smaller gain than the first IDAC and a full scale current that is less than the full scale current of the first IDAC.

23. A mixed signal processor for processing digital data and providing that data to an output as analog data in the analog domain, comprising the steps of:

a central processing unit (CPU) for processing digital data;

a first current Digital-to-Analog (IDAC) converter operable to convert a first digital value to a first current for output to a first output representing an analog value in the analog domain, the first IDAC having a first current step size associated with the Least Significant Bit (LSB) thereof;

a second IDAC operable to convert a second digital value to a second current for output to a second output representing an analog value in the analog domain, the second IDAC having a second current step size associated with the LSB thereof that is smaller than the first current step size;

a switching device for routing said first and second outputs to a first output node;

wherein the current through said first output node is the sum of the first and second currents;

wherein the combination of the first and second IDACs increases the bit resolution of said first IDAC when driving said first output node with the addition of said second IDAC.

24. The mixed signal processor of Claim 23, said switching device operable to inhibit said second IDAC from providing current to said first output node.

25. The mixed signal processor of Claim 23, wherein the outputs of the first and second steps of controlling are operable to Wire OR the outputs of both of the first and second IDACs to the first output node.

26. The mixed signal processor of Claim 25, wherein said switch is operable to selectively control said second IDAC to provide current to said first output node in a first and combination mode and to provide current to a second and separate output node in a second and non-combination mode.

27. The mixed signal processor of Claim 23, wherein said first and second IDACs drive

current to said first output node in a current sourcing operation.

28. The mixed signal processor of Claim 23, wherein at least one of said first and second IDACs is operable to sink current from said first output node.

29. The mixed signal processor of Claim 23, wherein said first and second IDACs each have a length "n" with there being 2^n levels of current separated by the first current size and second current size, respectively.

30. The mixed signal processor of Claim 29, wherein the combination of said first and second IDACs provides a combined IDAC with a length of $n + \log_2(m)$, wherein m is equal to the ratio of the first step size to the second step size.

31. The mixed signal processor of Claim 29, wherein said second IDAC has a smaller gain than said first IDAC.

32. The mixed signal processor of Claim 29, wherein said second IDAC has a full scale current that is less than the full scale current of said first IDAC.

33. The mixed signal processor of Claim 29, wherein said second IDAC has a smaller gain than the said IDAC and a full scale current that is less than the full scale current of said first IDAC.